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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/984,563	12/03/97	MAILLOUX J	95-0653.03

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EXAMINER	
KIM,H	
ART UNIT	**PAPER NUMBER**
2751	15

DATE MAILED: 04/25/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/984,563	Mailloux et al,
Examiner	**Group Art Unit**
H. Kim	2751

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 3/6/00.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 36-39, 59-69 is/are pending in the application.

Of the above claim(s)____ is/are withdrawn from consideration.

☐ Claim(s)____ is/are allowed.

☒ Claim(s) 36-39 + 59-69 is/are rejected.

☐ Claim(s)____ is/are objected to.

☐ Claim(s)____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s).____

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other____

Office Action Summary

Detailed Action

1. Claims 36-69 are presented for examination. This office action is in response to the Amendment filed on 3/6/00.

2. It is noted that this application appears to claim subject matter disclosed in the co-pending section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending applications to avoid possible double patenting.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 36-39 and 59-62 are rejected under 35 USC 102(b) as being anticipated by *Manning*, U.S. Patent 5,610,864.

As to claim 59, *Manning* discloses a method of accessing a memory (Fig. 1), comprising: receiving an external row address (Fig. 1 and Fig. 2, ADDR, ROW); choosing

whether the memory is in burst (col. 6 lines 14-26 and col. 7 lines 43-54) or a pipelined mode of operation (col. 5 lines 43-50); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and executing a read or write operation (Fig. 2, /WE).

As to claim 60, *Manning* further discloses switching between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipeline mode (col. 5 lines 43-50).

As to claims 61, *Manning* further discloses switching between a read and a write operations (Fig. 2 /WE).

As to claim 62, *Manning* further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

As to claim 36, *Manning* discloses the invention as claimed. *Manning* discloses a method for accessing an asynchronously access memory (Fig. 1 and EDO constitutes asynchrous memory, col. 6 lines 14-16), comprising the steps of: receiving an external row address to the asynchronously accessible dynamic random access memory accessible storage device (Fig. 1 and Fig. 2, ADDR, ROW); selecting between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50); selecting between a read and a write operation

(Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation);

obtaining a first external column address (Fig. 1 and Fig. 2, ADDR, COLm).

As to claim 37, *Manning* further discloses the step of obtaining a second external column address subsequent to the first external column address for operation in the pipeline mode (col. 5 lines 43-45)

As to claims 38, *Manning* further discloses generating internal address (col. 5 lines 51-62 and col. 8 line 67).

As to claims 39, *Manning* further discloses selecting path way (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not

commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 63-69 are rejected under 35 USC § 103(a) as being unpatentable over *Manning*, U.S. Patent 5,610,864 in view of *Ryan*, U.S. Patent 5,966,724 or *Rosich et al. (Rosich)*, U.S. Patent 5,587,964.

As to claim 65, *Manning* discloses a method of operating a memory circuit, comprising: receiving a mode select signal(col. 6 lines 14-34); receiving an initial external address (Fig. 1 and Fig. 2, ADDR); selecting a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); cycling a second enabling signal (Fig. 2 /CAS) ; generating an internal address (Fig. 1 Ref. 26); and receiving an external address on each cycle of the second enabling (col. 5 lines 43-49, "one access per cycle" read on this limitation). Although Manning discloses changing the mode and pipeline mode and, Manning does not specifically disclose a step of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state.

Ryan discloses the step of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state (Fig. 6, RAS and col. 8 lines 30-33) and receiving an external address on each cycle of the second enabling signal (Fig. 6 Ref. Addr) because it would allow the memory to switch mode of operation instantly thereby put the memory in high data throughput by eliminating the set up time (abstract lines 8-9).

One skilled in the art would have realized that maintaining a first enabling signal in active state would allow that the memory is always in ready to switch mode of operation thereby

increasing the access speed of the memory.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state of Ryan in the invention of Manning because it would allow the memory to switch mode of operation thereby increasing the memory access speed. The advantage of increasing the memory speed provide sufficient suggestion and motivation to one of ordinary skill in the memory art to follow the teaching of Ryan into invention of Manning.

Alternatively, Rosich discloses the step of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state (col. 8 lines 24-48 and RASL in Fig. 7, Ref. 700, page mode & 710, burst mode) for the purpose of reducing memory access time and component latency by enabling the memory chip throughout the operations (col. 1 lines 21-31).

One of ordinary skill in the art familiar with Manning, and looking at Rosich would have recognized that the memory access cycle of Manning would have been reduced by maintaining a first enabling signal in active state during mode of operations because it would provide capability of that the memory is always in ready to receive a mode command thereby increasing the access speed of the memory. Increasing memory speed would have a highly desirable feature in the computer system environment of Rosich because the objective of computer system is increasing speed or computing power.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of maintaining a first enabling signal in active state of Rosich in the invention of Manning because it would increase memory access speed of Manning by providing capability of that the memory is always in ready to receive a command. *Rosich* further discloses switching the mode select signal to select a first mode while maintaining the first enabling signal in the active state and changing the mode select signal to select a second mode (col. 8 lines 24-48 and Fig. 7, Refs. 700 & 710).

As to claim 66, *Manning, Ryan, and Rosich* disclose the calms as the above claim 65. Manning further discloses a step of maintaining a mode select signal to select a burst mode of operation (Fig. 2 /OE, col. 7 lines 45-55 & col. 6 lines 14+) and switching the mode to a pipelined mode on successive cycles of the second enabling signal by changing the mode select signal (col. 5 lines 43-49, "one access per cycle" read on this limitation). Ryan and Rosich discloses a step of switching the mode on the successive cycles of the second enabling signal (Fig. 6, RAS and col. 8 lines 30-33 in Ryan and col. 8 lines 24-48 and Fig. 7, Refs. 700 & 710 in Rosich).

As to claim 67, *Manning* further discloses the step of maintaining a mode select signal to select a burst mode of operation (Col. 6 lines 14-34); receiving a stream of addresses and a cycling a second enabling signal (Fig. 2 /CAS); changing the mode select signal to select a

pipelined mode of operation (col. 5 lines 43-50).

As to claim 68, *Manning* further discloses the steps of selecting a pipeline mode (col. 5 lines 43-49); select an external address only path when the pipeline mode is selected (col. 5 lines 43-49, "one access per cycle" read on this limitation); and selecting an internal buffered external address path (col. 4 lines 23-48) and generating internal column address (col. 8 line 67) when the burst mode of operation is selected.

As to claims 63 and 69, *Manning* further discloses an external address only path for the pipeline mode (col. 5 lines 43-49, "one access per cycle" read on this limitation); an internal buffered external address path for the burst mode of operation (col. 4 lines 23-48 & col. 8 line 67); and pipeline (col. 5 lines 41-50)/burst circuitry (col. 6 lines 14-26 and col. 7 lines 43-54) .

As to claim 64, *Manning* further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col. 6 lines 14+).

Response to Amendment

6. Applicant's arguments with respect to claims 36-39, 59-62, and 63-69 have been considered but are deemed to be moot in view of the new grounds of rejection.

Applicant's remarks on page 3 concerning the references not teaching switching between a

burst mode and pipeline mode is not considered persuasive. Manning discloses this limitation (col. 5 lines 43-47 and col. 7 lines 44-55, "the current invention include a pipelined architecture" and "switching between standard fast page mode (non-EDO) and burst mode" read on this limitation, in other words, Manning discloses switching between fast page pipeline and burst pipeline See also, Fig. 2 and col. 6 lines 14-22). Ryan also discloses the step of switching between a burst mode and pipeline mode (col. 4 line 24- 28).

Applicant's argument on page 4 that the reference does not disclose selecting an external address and an initial buffered external address path is not considered persuasive. Manning discloses an external address (col. 4 lines 23+ and col. 5 lines 43-49, "one access per cycle"); and initial buffered external address (col. 4 lines 23-48 & col. 8 line 67).

Applicant's remarks on page 4 concerning the references not teaching maintenance of signals of enabling is not considered persuasive. Manning discloses this limitation (col. 7. Lines 45-47 and Fig. 2. /OE (mode select signal) when the power is on (first enable signal) reads on this limitation). Ryan discloses maintenance of signals of enabling (Fig. 6, RAS and col. 8 lines 30-33) because it would allow the memory to switch mode of operation instantly thereby put the memory in high data throughput by eliminating the set up time (abstract lines 8-9). Rosich also discloses maintenance of signals of enabling (col. 8 lines 24-48 and Fig. 7, Refs. 700 & 710) for the purpose of reducing memory access time and component latency by enabling the memory chip throughout the operations (col. 1 lines 21-31). Therefore broadly written claims are disclosed by the references cited.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US 5966724, 19991012, Synchronous memory device with dual page and burst mode operations, Ryan, Kevin J..
2. US 5587964, 19961224, Page mode and nibble mode DRAM, Rosich, Mitchell N. , et al.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

10. When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

11. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

12. When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

14. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051-2, (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Patent Examiner
April 18, 2000

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER